CLAIMS

What is claimed is:

1. An image processing system, comprising:

a deterministic prediction decode unit for predicting individual pixels of an image based on a predetermined deterministic prediction algorithm, the deterministic prediction decode unit comprising:

a look-up table for storing values to be used by the predetermined deterministic prediction algorithm when converting a relatively low resolution image to a relatively higher resolution image;

wherein the look-up table is organized into four spatial phases, and wherein a prediction is made for a target pixel by accessing at least two of the four spatial phases of the look-up table to read at least two possible values of the target pixel.

2. The image processing system of claim 1, wherein the look-up table is implemented in a memory device, and a plurality of reference pixels are provided for addressing the memory device to retrieve the values to be used by the predetermined deterministic prediction algorithm, wherein a reference pixel is a pixel that is used to predict a value of the target pixel.

3. The image processing system of claim 2, wherein the memory device comprises first, second, third, and fourth memory portions corresponding to first, second, third, and fourth spatial phases, respectively, and the second memory portion is divided into first and second sub-portions, wherein values are stored in the first and second sub-portions based on a predetermined bit of the reference pixels used to access the first and second sub-portions.

4. The image processing system of claim 3, further comprising:

a first multiplexer having a first input coupled to an output of the first sub-portion for receiving second phase prediction values, a second input coupled to an output of the second sub-portion for receiving the second phase prediction values, and an output for providing a second phase prediction result; and

a second multiplexer having a first input coupled to an output of the first memory portion for receiving a first phase prediction value, a second input for receiving a first phase pixel value from another source, and an output coupled to a control input of the first multiplexer, the output of the second multiplexer for providing a first phase decoded pixel value.

5. The image processing system of claim 4, wherein the fourth memory is divided into third and fourth sub-portions, wherein values are stored in

the third and fourth sub-portions based on a predetermined bit of the reference pixels used to access the third and fourth sub-portions.

6. The image processing system of claim 5, further comprising:

a third multiplexer having a first input coupled to an output of the third sub-portion for receiving fourth prediction values, a second input coupled to an output of the fourth sub-portion for receiving the fourth phase prediction values, and an output for providing a fourth phase prediction result; and

a fourth multiplexer having a first input coupled to an output of the third memory portion for receiving a third phase prediction value, a second input for receiving a third phase pixel value from another source, and an output coupled to a control input of the third multiplexer, the output of the fourth multiplexer for providing a third phase decoded pixel value.

7. The image processing system of claim 6, wherein if the first phase prediction value is determined to be predictable using deterministic prediction, the second phase prediction result is provided within a same clock period.

8. The image processing system of claim 7, wherein if the first phase prediction value is determined to be not predictable using deterministic prediction, the second phase prediction result is provided within a same

clock period that the first phase pixel value is available to the second multiplexer.

9. The image processing system of claim 8, wherein if the third phase prediction value is determined to be predictable using deterministic prediction, the fourth phase prediction result is provided within a same clock period.

10. The image processing system of claim 9, wherein if the third phase prediction value is determined to be not predictable using deterministic prediction, the fourth phase prediction result is provided within a same clock period that the third phase pixel value is available to the third multiplexer.

11. A method for deterministic prediction of a target pixel in an image processing system, comprising the steps of:

providing reference pixels corresponding to the target pixel to address terminals of first and second memories;

storing prediction values in the first and second memories based on a predetermined bit of the reference pixels; and

retrieving the prediction values from the first and second memories in response to the reference pixels for providing two prediction values corresponding to the target pixel.

12. The method of claim 11, wherein the predetermined bit is characterized as being a most significant bit of the reference pixels used to access the first and second memories.

13. The method of claim 11, further comprising the steps of:

determining that the first and second memories store second phase prediction values;

storing first phase prediction values in a third memory;

retrieving the first phase prediction value for a first phase target pixel;

if the first phase prediction value is predictable, the first phase prediction value determines a first phase decoded pixel value, and the first phase decoded pixel value is used to select one of the two second phase prediction values as a second phase prediction result.

14. The method of claim 13, further comprising the step of:

if the first phase prediction value is not predictable, the first phase decoded pixel value is determined by another source, and the first phase decoded pixel value is used to select one of the two second phase prediction values as a second phase prediction result.

15. The method of claim 13, wherein if the first phase prediction value is determined to be predictable, the second phase prediction result is provided within a same clock period as the first phase prediction value is determined.

16. An image processing system, comprising:

an adaptive arithmetic decoder for receiving compressed image data, and in response, providing high resolution data;

a higher resolution image buffer for receiving the high resolution data, and in response, providing a first plurality of reference pixels;

a deterministic prediction decode unit, for receiving the first plurality of reference pixels and a second plurality of reference pixels, the deterministic prediction decode unit comprising:

a look-up table for storing values to be used by a deterministic prediction algorithm when converting a relatively low resolution image to a relatively higher resolution image;

wherein the look-up table is organized into four spatial phases, and wherein a prediction is made for a target pixel by accessing at least two of the four spatial phases of the look-up table to read at least two possible values of the target pixel.

17. The image processing system of claim 16, wherein the look-up table is implemented in a memory device, and the first and second pluralities of reference pixels are provided for addressing the memory device to retrieve the values to be used by the deterministic prediction algorithm, wherein a reference pixel is a pixel that is used to predict a value of the target pixel.

18. The image processing system of claim 17, wherein the memory device comprises first, second, third, and fourth memory portions corresponding to first, second, third, and fourth spatial phases, respectively, and the second memory portion is divided into first and second sub-portions, wherein values are stored in the first and second sub-portions based on a predetermined bit of the reference pixels used to access the first and second sub-portions.

19. The image processing system of claim 18, further comprising:

a first multiplexer having a first input coupled to an output of the first sub-portion for receiving second phase prediction values, a second input coupled to an output of the second sub-portion for receiving the second phase prediction values, and an output for providing a second phase prediction result; and

a second multiplexer having a first input coupled to an output of the first memory portion for receiving a first phase prediction value, a second input for receiving a first phase

pixel value from another source, and an output coupled to a control input of the first multiplexer, the output of the second multiplexer for providing a first phase decoded pixel value.

20. The image processing system of claim 19, wherein if the first phase prediction value is determined to be predictable using deterministic prediction, the second phase prediction result is provided within a same clock period.